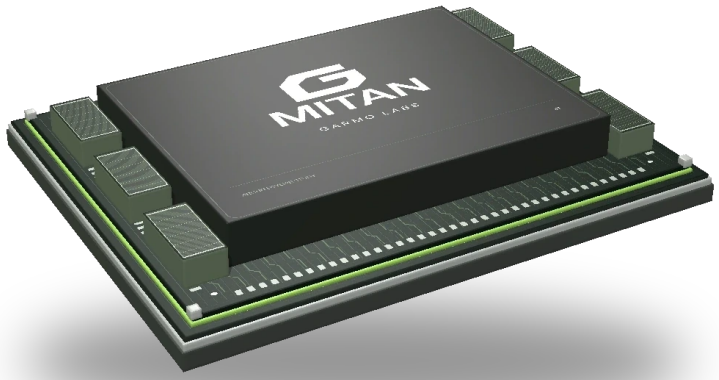
SEMANTIC AI & REASONING

MITAN-X1

Semantic memory, reasoning and specialized compute in one integrated architecture—coordinating AI workloads with power policy, trusted control and dataflow.



Architectural concept. Not a die photograph, physical layout or measured device.

IP-4677 · Source + model · RTL + reference models

Function and architecture

- Semantic-memory and migration control
- Dedicated reasoning and compute-fusion tiles
- Power/resource orchestration and trust/RAS
- Shared SoC substrate with a universal accelerator plane

Integration summary

The flagship joins semantic-memory, solver/reasoning, compute-fusion and semantic-transport tiles to a shared SoC substrate. Peripherals, reliable digital links and host interfaces are part of the integration scope. Process-specific PHYs, clocking, pads and package implementation require separately qualified collateral.

Technical record

Canonical identity	IP-4677
Responsibility	Semantic memory, reasoning and specialized compute in one integrated architecture—coordinating AI workloads with power policy, trusted control and dataflow.
Delivery boundary	RTL + reference models
Evidence scope	Source + model

Delivery and release binding

- Exact SoC/top and configuration
- Clock, reset, power and pad contract
- Memory, PHY and package dependencies
- Release-specific PVT and signoff views

Confirm for the selected release: Node/library binding, Clock/reset limits, Physical and protocol dependencies, Artifact hashes, Acceptance criteria.

Evidence and qualification

Our records show source integration, controlled donor provenance and executed architecture/reference-model campaigns. Integrated SoC HDL, synthesis, formal, DFT and physical qualification remained pending at the recorded cutoff.

Reference-model results are not full-SoC signoff or measured silicon. The exact integrated release and target-node evidence control any physical delivery or performance claim.

Canonical status: SOURCE IMPLEMENTED / REFERENCE EVIDENCE / INTEGRATED CAD CLOSURE PENDING

Evaluation and licensing

Evaluation: Architecture and release evaluation. Production: Chip / SoC licensing program. Custom work: Custom silicon integration. Rights, pricing, support and acceptance criteria are agreed for the exact scope.

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