PROCESSOR / SYSTEM ARCHITECTURE

RASIN

An upward-compatible architectural root spanning embedded, real-time, client, server and AI/HPC implementations.



Architectural concept. Not a die photograph, physical layout or measured device.

IP-3672 · RTL + models · Architecture + RTL

Function and architecture

- Upward-compatible architectural root
- Embedded and real-time implementation classes
- Client, server and AI/HPC implementation classes
- Conventional compiled-programming model

Integration summary

Select the RASIN implementation class and confirm its supported compiled-programming, memory and runtime contracts. Bind peripherals and physical views for that release. Recorded digital/formal closure is preserved separately from the outstanding physical-signoff stage.

Technical record

Canonical identity	IP-3672
Responsibility	One upward-compatible architectural root spanning embedded, real-time, client, server and AI/HPC implementations while preserving conventional compiled programming models.
Delivery boundary	Architecture + RTL
Evidence scope	RTL + models

Delivery and release binding

- Exact SoC/top and configuration
- Clock, reset, power and pad contract
- Memory, PHY and package dependencies
- Release-specific PVT and signoff views

Confirm for the selected release: Node/library binding, Clock/reset limits, Physical and protocol dependencies, Artifact hashes, Acceptance criteria.

Evidence and qualification

The later RASIN record reports digital/formal closure, with the physical-signoff stage remaining open.

Node-specific physical implementation and system qualification are scoped separately.

Canonical status: P1 / IMPLEMENTATION-BACKED ARCHITECTURE

Evaluation and licensing

Evaluation: Architecture and release evaluation. Production: Chip / SoC licensing program. Custom work: Custom silicon integration. Rights, pricing, support and acceptance criteria are agreed for the exact scope.

Contact: patrick@garmolabs.com | Product path: /silicon/rasin