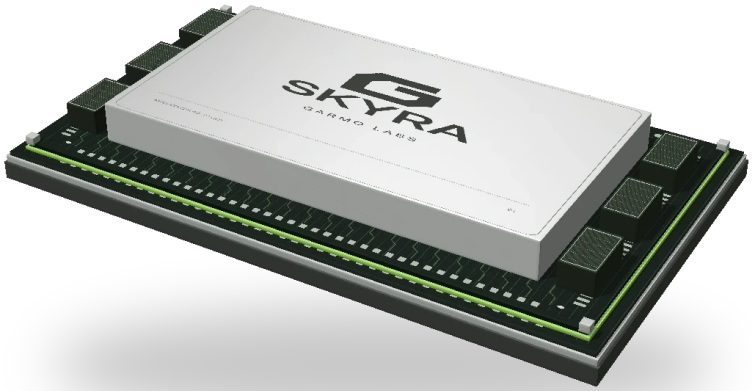
CAPABILITY DATAFLOW

# SKYRA

Block-atomic explicit dataflow and capability-native memory bring execution, commit and access authority into the processor architecture.




Architectural concept. Not a die photograph, physical layout or measured device.

IP-2574 · RTL + models · Architecture + RTL

## Function and architecture

- Block-Atomic Explicit Dataflow
- Capability-native protected memory
- Dense, sparse and vector acceleration
- Homogeneous fabric-tile architecture

## Integration summary

Producer–consumer dataflow executes inside block-atomic hyperblocks. Capability metadata governs memory access, with a SKY130 proof-top path distinct from full-scale fabric targets.

## Technical record

| | |
|---|---|
| **Canonical identity** | IP-2574 |
| **Responsibility** | Block-Atomic Explicit Dataflow + native capability-memory processor architecture with homogeneous SFT integration, dense+sparse/vector acceleration, security and node/package abstraction. |
| **Delivery boundary** | Architecture + RTL |
| **Evidence scope** | RTL + models |

## Delivery and release binding

- Exact SoC/top and configuration
- Clock, reset, power and pad contract
- Memory, PHY and package dependencies
- Release-specific PVT and signoff views

Confirm for the selected release: Node/library binding, Clock/reset limits, Physical and protocol dependencies, Artifact hashes, Acceptance criteria.

## Evidence and qualification

Implementation-backed architecture and source are recorded. Later records show an AWS-validated repair of the SKYRA M0 SKY130 capability/security path.

The source repair does not create a new physical-signoff or returned-silicon claim.

Canonical status: P1 / IMPLEMENTATION-BACKED ARCHITECTURE

## Evaluation and licensing

Evaluation: Architecture and release evaluation. Production: Chip / SoC licensing program. Custom work: Custom silicon integration. Rights, pricing, support and acceptance criteria are agreed for the exact scope.

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