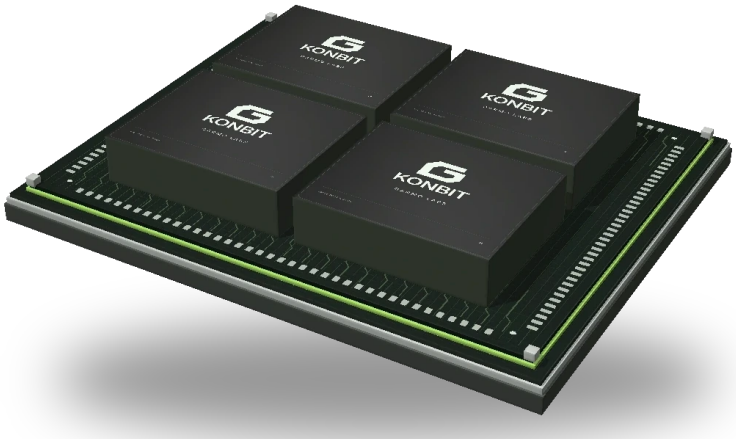
AI + HPC

KONBIT-X1

A heterogeneous accelerator family that treats compute, state, optimization and fabric as collaborating parts of one machine.



Architectural concept. Not a die photograph, physical layout or measured device.

IP-233 · Architecture IP · Architecture

Function and architecture

- Compute, state and optimization tiles
- Training, reasoning and scientific configurations
- Trust and reliability tile classes
- Companion profiler, model and autotuner

Integration summary

KONBIT-X1 is the universal AI/HPC member of the KONBIT family. Its developer suite supports cycle-model exploration, deterministic replay and configuration tuning.

Technical record

Canonical identity	IP-233
Responsibility	KONBIT product architecture
Documented building blocks	universal AI/HPC accelerator
Delivery boundary	Architecture
Evidence scope	Architecture IP

Delivery and release binding

- Exact SoC/top and configuration
- Clock, reset, power and pad contract
- Memory, PHY and package dependencies
- Release-specific PVT and signoff views

Confirm for the selected release: Node/library binding, Clock/reset limits, Physical and protocol dependencies, Artifact hashes, Acceptance criteria.

Evidence and qualification

Architecture and reusable technology are recorded in the controlled catalog. Request the exact release evidence for your intended integration.

Developer-model performance is not measured chip PPA. Architecture, implementation and target-node evidence are qualified separately.

Canonical status: Engineering architecture/build target

Evaluation and licensing

Evaluation: Architecture and release evaluation. Production: Chip / SoC licensing program. Custom work: Custom silicon integration. Rights, pricing, support and acceptance criteria are agreed for the exact scope.

Contact: patrick@garmolabs.com | Product path: /silicon/konbit-x1