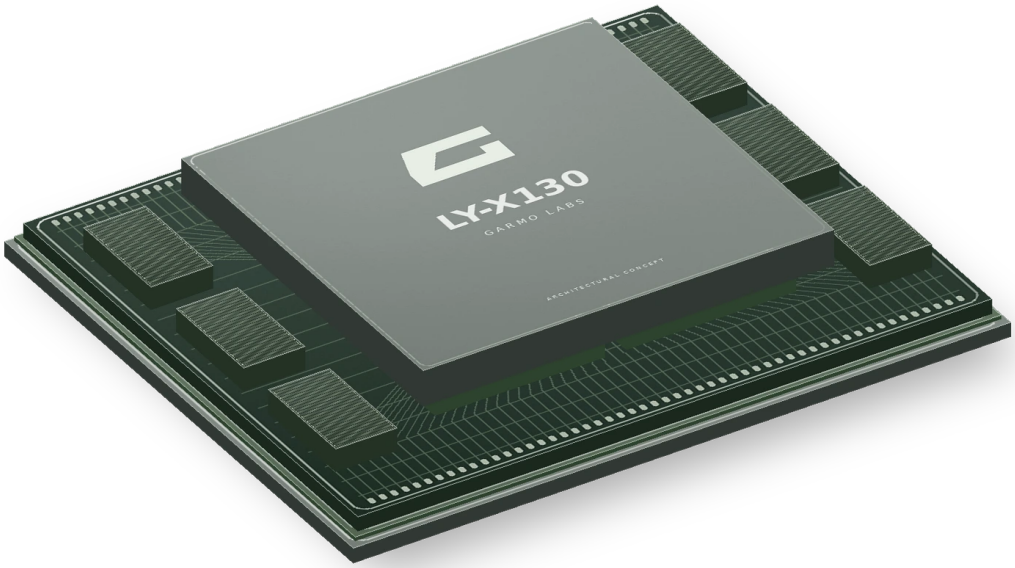
EXTREME-SCALE LY SUPERPROCESSOR

# LY-X130

The extreme-scale LY system architecture joins the full engine set with chiplet/fabric, HBM, collectives and runtime/compiler integration.




Architectural concept. Not a die photograph, physical layout or measured device.

IP-078 · Architecture IP · Architecture

## Function and architecture

- Full LY engine set
- chiplet/fabric
- HBM
- collectives

## Integration summary

Integrate the full LY engine set under its runtime/compiler interface and qualify HBM, chiplet/fabric and collective endpoints individually. Confirm security domains, RAS behavior, package assumptions and external hard-IP dependencies for the selected release.

## Technical record

| | |
|---|---|
| **Canonical identity** | IP-078 |
| **Responsibility** | Extreme-scale LY superprocessor |
| **Documented building blocks** | Full LY engine set; chiplet/fabric; HBM; collectives; runtime/compiler; RAS/security. |
| **Delivery boundary** | Architecture |
| **Evidence scope** | Architecture IP |

## Delivery and release binding

- Exact SoC/top and configuration
- Clock, reset, power and pad contract
- Memory, PHY and package dependencies
- Release-specific PVT and signoff views

Confirm for the selected release: Node/library binding, Clock/reset limits, Physical and protocol dependencies, Artifact hashes, Acceptance criteria.

## Evidence and qualification

Architecture and reusable technology are recorded in the controlled catalog. Request the exact release evidence for your intended integration.

Node-specific physical implementation and system qualification are scoped separately.

Canonical status: Engineering build-spec family

## Evaluation and licensing

Evaluation: Architecture and release evaluation. Production: Chip / SoC licensing program. Custom work: Custom silicon integration. Rights, pricing, support and acceptance criteria are agreed for the exact scope.

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