GENERAL REASONING/DATAFLOW AI SUPERPROCESSOR

LY-S130

A reasoning and dataflow AI architecture combining matrix/vector execution, attention, sequence state and graph/search resources.



Architectural concept. Not a die photograph, physical layout or measured device.

IP-071 · Architecture IP · Architecture

Function and architecture

- LY ISA and matrix/vector execution
- Attention, sequence and sparse engine roles
- KV state and graph/search resources
- Collectives and GarmoLink-LY integration

Integration summary

Map the workload to the supported LY ISA and runtime contract. Bind matrix/vector, attention, sequence, sparse and KV functions to the selected memory organization, then qualify collectives and GarmoLink-LY endpoints for that configuration.

Technical record

Canonical identity	IP-071
Responsibility	General reasoning/dataflow AI superprocessor
Documented building blocks	LY ISA; matrix/vector; attention; sequence; sparse; KV; graph/search; collectives; GarmoLink-LY.
Delivery boundary	Architecture
Evidence scope	Architecture IP

Delivery and release binding

- Exact SoC/top and configuration
- Clock, reset, power and pad contract
- Memory, PHY and package dependencies
- Release-specific PVT and signoff views

Confirm for the selected release: Node/library binding, Clock/reset limits, Physical and protocol dependencies, Artifact hashes, Acceptance criteria.

Evidence and qualification

Architecture and reusable technology are recorded in the controlled catalog. Request the exact release evidence for your intended integration.

Node-specific physical implementation and system qualification are scoped separately.

Canonical status: Engineering build-spec family

Evaluation and licensing

Evaluation: Architecture and release evaluation. Production: Chip / SoC licensing program. Custom work: Custom silicon integration. Rights, pricing, support and acceptance criteria are agreed for the exact scope.

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