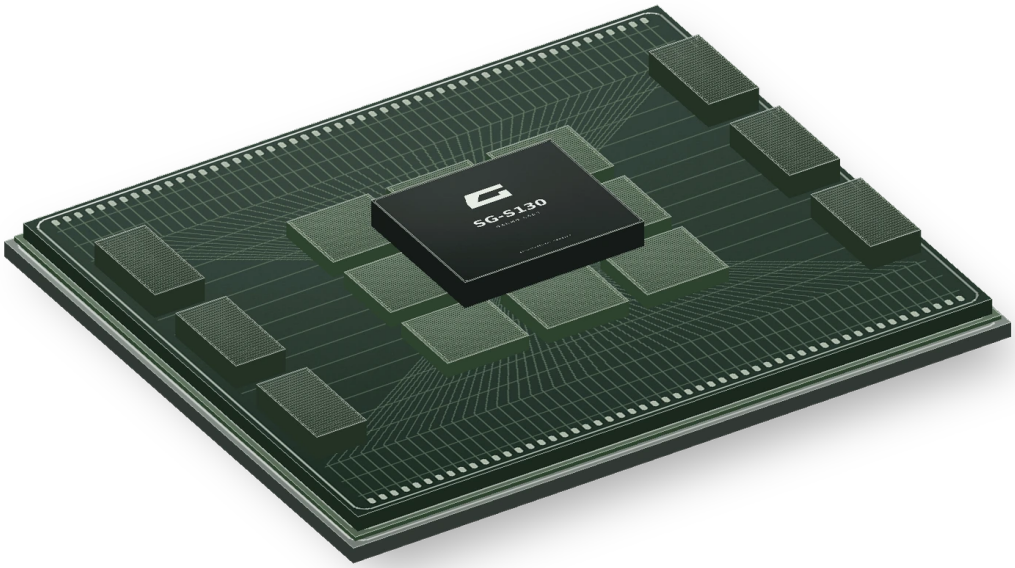
SPARSE / GRAPH / SOLVER SUPERCOMPUTER

SG-S130

A sparse, graph and solver architecture organized around SG tiles, local engines and a shared fabric.



Architectural concept. Not a die photograph, physical layout or measured device.

IP-063 · Architecture IP · Architecture

Function and architecture

- SG tiles
- graph engines
- solver engines
- sparse/tensor assist

Integration summary

Bind RISC-V control, SG tile interfaces and the chosen graph/solver engines to SGFabric. Confirm the SGLink endpoint contract, memory service, clock/reset assumptions and supported configuration for the selected release before top-level integration.

Technical record

Canonical identity	IP-063
Responsibility	Sparse / graph / solver supercomputer
Documented building blocks	SG tiles; graph engines; solver engines; sparse/tensor assist; SGFabric; SGLink; RISC-V control.
Delivery boundary	Architecture
Evidence scope	Architecture IP

Delivery and release binding

- Exact SoC/top and configuration
- Clock, reset, power and pad contract
- Memory, PHY and package dependencies
- Release-specific PVT and signoff views

Confirm for the selected release: Node/library binding, Clock/reset limits, Physical and protocol dependencies, Artifact hashes, Acceptance criteria.

Evidence and qualification

Architecture and reusable technology are recorded in the controlled catalog. Request the exact release evidence for your intended integration.

Node-specific physical implementation and system qualification are scoped separately.

Canonical status: Engineering build-spec family

Evaluation and licensing

Evaluation: Architecture and release evaluation. Production: Chip / SoC licensing program. Custom work: Custom silicon integration. Rights, pricing, support and acceptance criteria are agreed for the exact scope.

Contact: patrick@garmolabs.com | Product path: /silicon/sg-s130