MEMORY & COHERENCY

vXPU Photonic Cognitive Fabric

Integrated digital control plane, tenant/WDM allocation, configuration ownership/epochs, scheduling, fault quarantine, ECC, telemetry, Morph compiler, behavioral PCM/MZI/WDM/thermal models, abstract 128x128 photonic GDS generation and verification/signoff harnesses.

IP-4379 · Source / reference evidence · RTL / reference evaluation

Function and architecture

• Integrated digital control plane, tenant/WDM allocation, configuration ownership/epochs, scheduling, fault quarantine, ECC, telemetry, Morph compiler, behavioral PCM/MZI/WDM/thermal models, abstract 128x128 photonic GDS generation and verification/signoff harnesses.

Integration summary

vXPU Photonic Cognitive Fabric provides the documented photonic compute / multi-tenant accelerator-fabric engineering ip responsibility: Integrated digital control plane, tenant/WDM allocation, configuration ownership/epochs, scheduling, fault quarantine, ECC, telemetry, Morph compiler, behavioral PCM/MZI/WDM/thermal models, abstract 128x128 photonic GDS generation and verification/signoff harnesses. Evaluate the exact VXPU-PCF-001 implementation and confirm its integration contract before using it inside the target design.

Technical record

Canonical identity	IP-4379
Native implementation identity	VXPU-PCF-001
Documented responsibility	Integrated digital control plane, tenant/WDM allocation, configuration ownership/epochs, scheduling, fault quarantine, ECC, telemetry, Morph compiler, behavioral PCM/MZI/WDM/thermal models, abstract 128x128 photonic GDS generation and verification/signoff harnesses.
Recorded evidence class	Source / reference evidence
Interface and physical parameters	Bound to the selected source/configuration; not inferred from name or family.

Delivery and release binding

• Exact implementation and configuration manifest

• Documented interfaces and clock/reset contract

- Available reference or verification collateral
- Recorded physical views where authorized and applicable
- Integration acceptance criteria and unresolved gate list

Confirm for the selected release: Source/configuration identity, Interface and dependencies, Verification evidence, Process/library where applicable, Authorized package and acceptance criteria.

Evidence and qualification

local tests PASS; full 128x128 GDS generated and independently structurally parsed; release record and deterministic ZIP hash recorded; HDL gauntlet source present.

Evidence shown is our record for this canonical implementation, not a fresh tool rerun. External foundry acceptance, silicon measurements, standards certification and unlisted interface/physical parameters are not inferred. Exact delivery and rights are agreed before licensing.

Canonical status: P2 HETEROGENEOUS ENGINEERING RELEASE: SOFTWARE/MODEL + ABSTRACT-GDS STRUCTURAL EVIDENCE EXECUTED; HDL SIM/LINT/SYNTH/FORMAL NOT RUN AT SEALED IMPORT; PHOTONIC PDK/DEVICE/FOUNDRY/SILICON SIGNOFF OPEN.

Evaluation and licensing

Evaluation: Review the exact recorded implementation and agreed test scope. Production: Named-design rights for the agreed qualified release. Custom work: Target integration, verification or physical qualification. Rights, pricing, support and acceptance criteria are agreed for the exact scope.

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