COMPUTE & AI

NPJ SolveTile v1.0.0

Reusable solver/bitset/sparse tile binding lane ALU, popcount/zero-skip, descriptor FIFO and deterministic transport to a reference model and SV source.

IP-4276 · RTL + models · Soft IP / model

Function and architecture

- Reusable solver/bitset/sparse tile binding lane ALU
- popcount/zero-skip
- descriptor FIFO and deterministic transport to a reference model and SV source

Integration summary

NPJ SolveTile v1.0.0 addresses reusable solver/bitset/sparse tile binding lane ALU, popcount/zero-skip, descriptor FIFO and deterministic transport to a reference model and SV source.

Technical record

Canonical identity	IP-4276
Responsibility	Reusable solver/bitset/sparse tile binding lane ALU, popcount/zero-skip, descriptor FIFO and deterministic transport to a reference model and SV source.
Delivery boundary	Soft IP / model
Evidence scope	RTL + models

Delivery and release binding

- Interface version and parameter set
- Clock/reset domains and integration constraints
- Companion memory, PHY and software requirements
- Verification collateral and acceptance criteria

Confirm for the selected release: Node/library binding, Clock/reset limits, Physical and protocol dependencies, Artifact hashes, Acceptance criteria.

Evidence and qualification

Our records show source/model or productization evidence for this IP. The selected HDL, verification and physical views are reviewed per release.

No node-port, silicon-performance, standards certification or analog qualification is inherited from a related product.

Canonical status: P1-P2 / SOURCE + MODEL TESTS; REMOTE HDL/SYNTH/P&R NOT_RUN

Evaluation and licensing

Evaluation: Evaluate an individual IP configuration. Production: Named-design production license. Custom work: Node binding or derivative integration. Rights, pricing, support and acceptance criteria are agreed for the exact scope.

Contact: patrick@garmolabs.com | Product path: /ip/npj-solvetile-v1-0-0