INTERCONNECT & NETWORKING

GHSI High-Speed Interconnect Architecture

Digital reliable-link architecture covering CRC integrity, sequencing, retry/replay, parameterized width, lane-fabric hooks and a physical proof top below higher-level GFI/GACF transports.

IP-4215 · Source / reference evidence · RTL / reference evaluation

Function and architecture

• Digital reliable-link architecture covering CRC integrity, sequencing, retry/replay, parameterized width, lane-fabric hooks and a physical proof top below higher-level GFI/GACF transports.

Integration summary

GHSI High-Speed Interconnect Architecture provides the documented high-speed interconnect / link architecture responsibility: Digital reliable-link architecture covering CRC integrity, sequencing, retry/replay, parameterized width, lane-fabric hooks and a physical proof top below higher-level GFI/GACF transports. Evaluate the exact GHSI-IP-001 implementation and confirm its integration contract before using it inside the target design.

Technical record

Canonical identity	IP-4215
Native implementation identity	GHSI-IP-001
Documented responsibility	Digital reliable-link architecture covering CRC integrity, sequencing, retry/replay, parameterized width, lane-fabric hooks and a physical proof top below higher-level GFI/GACF transports.
Recorded evidence class	Source / reference evidence
Interface and physical parameters	Bound to the selected source/configuration; not inferred from name or family.

Delivery and release binding

• Exact implementation and configuration manifest

• Documented interfaces and clock/reset contract

• Available reference or verification collateral

• Recorded physical views where authorized and applicable

• Integration acceptance criteria and unresolved gate list

Confirm for the selected release: Source/configuration identity, Interface and dependencies, Verification evidence, Process/library where applicable, Authorized package and acceptance criteria.

Evidence and qualification

Evidence retained in our records

Evidence shown is our record for this canonical implementation, not a fresh tool rerun. External foundry acceptance, silicon measurements, standards certification and unlisted interface/physical parameters are not inferred. Exact delivery and rights are agreed before licensing.

Canonical status: P1 / SOURCE-BACKED DIGITAL LINK ARCHITECTURE; FULL CI CURRENTLY FAILING; PHYSICAL OPEN

Evaluation and licensing

Evaluation: Review the exact recorded implementation and agreed test scope. Production: Named-design rights for the agreed qualified release. Custom work: Target integration, verification or physical qualification. Rights, pricing, support and acceptance criteria are agreed for the exact scope.

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