MEMORY & COHERENCY

SONJE Reliability / RAS Memory Architecture

Defines ECC, poison, scrub, remap/spare interfaces and media-specific telemetry hooks while keeping silicon retention/disturb/wear claims at foundry/vendor characterization boundaries.

IP-3898 · Executed digital evidence · RTL / reference evaluation

Function and architecture

• Defines ECC, poison, scrub, remap/spare interfaces and media-specific telemetry hooks while keeping silicon retention/disturb/wear claims at foundry/vendor characterization boundaries.

Integration summary

SONJE Reliability / RAS Memory Architecture provides the documented memory reliability architecture responsibility: Defines ECC, poison, scrub, remap/spare interfaces and media-specific telemetry hooks while keeping silicon retention/disturb/wear claims at foundry/vendor characterization boundaries. Evaluate the exact SONJE-IP-022 implementation and confirm its integration contract before using it inside the target design.

Technical record

Canonical identity	IP-3898
Native implementation identity	SONJE-IP-022
Documented responsibility	Defines ECC, poison, scrub, remap/spare interfaces and media-specific telemetry hooks while keeping silicon retention/disturb/wear claims at foundry/vendor characterization boundaries.
Recorded evidence class	Executed digital evidence
Interface and physical parameters	Bound to the selected source/configuration; not inferred from name or family.

Delivery and release binding

• Exact implementation and configuration manifest

• Documented interfaces and clock/reset contract

• Available reference or verification collateral

• Recorded physical views where authorized and applicable

• Integration acceptance criteria and unresolved gate list

Confirm for the selected release: Source/configuration identity, Interface and dependencies, Verification evidence, Process/library where applicable, Authorized package and acceptance criteria.

Evidence and qualification

Evidence retained in our records

Evidence shown is our record for this canonical implementation, not a fresh tool rerun. External foundry acceptance, silicon measurements, standards certification and unlisted interface/physical parameters are not inferred. Exact delivery and rights are agreed before licensing.

Canonical status: P1 / P64 512-BIT ECC + MBIST/BISR IMPLEMENTATION; RTL/FORMAL/SYNTHESIS GATES OBSERVED PASS; FULL PRODUCTION RAS/DFT OPEN

Evaluation and licensing

Evaluation: Review the exact recorded implementation and agreed test scope. Production: Named-design rights for the agreed qualified release. Custom work: Target integration, verification or physical qualification. Rights, pricing, support and acceptance criteria are agreed for the exact scope.

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