AI & TENSOR COMPUTE

KOURAN Morphable Compute Lattice Architecture

One morphable PE lattice is intended to map dense matrix, sparse tensor, vector, reduction, graph and solver/search primitives rather than separate fixed-function dense/sparse islands.

IP-3645 · Source / reference evidence · RTL / reference evaluation

Function and architecture

• One morphable PE lattice is intended to map dense matrix, sparse tensor, vector, reduction, graph and solver/search primitives rather than separate fixed-function dense/sparse islands.

Integration summary

KOURAN Morphable Compute Lattice Architecture provides the documented ai / hpc / general compute architecture responsibility: One morphable PE lattice is intended to map dense matrix, sparse tensor, vector, reduction, graph and solver/search primitives rather than separate fixed-function dense/sparse islands. Evaluate the exact KOURAN-IP-015 implementation and confirm its integration contract before using it inside the target design.

Technical record

Canonical identity	IP-3645
Native implementation identity	KOURAN-IP-015
Documented responsibility	One morphable PE lattice is intended to map dense matrix, sparse tensor, vector, reduction, graph and solver/search primitives rather than separate fixed-function dense/sparse islands.
Recorded evidence class	Source / reference evidence
Interface and physical parameters	Bound to the selected source/configuration; not inferred from name or family.

Delivery and release binding

• Exact implementation and configuration manifest

• Documented interfaces and clock/reset contract

• Available reference or verification collateral

• Recorded physical views where authorized and applicable

• Integration acceptance criteria and unresolved gate list

Confirm for the selected release: Source/configuration identity, Interface and dependencies, Verification evidence, Process/library where applicable, Authorized package and acceptance criteria.

Evidence and qualification

Architecture docs + morphable PE + 4x4 mesh RTL.

Evidence shown is our record for this canonical implementation, not a fresh tool rerun. External foundry acceptance, silicon measurements, standards certification and unlisted interface/physical parameters are not inferred. Exact delivery and rights are agreed before licensing.

Canonical status: P1 / IMPLEMENTATION-BACKED ARCHITECTURE; FULL 64-PE TILE NOT PRESENT

Evaluation and licensing

Evaluation: Review the exact recorded implementation and agreed test scope. Production: Named-design rights for the agreed qualified release. Custom work: Target integration, verification or physical qualification. Rights, pricing, support and acceptance criteria are agreed for the exact scope.

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