CPU & EXECUTION

KX RISC-V Branch Prediction

Digital RTL implementation indexed as kx_riscv_bpu. The recorded role is risc-v branch prediction; exact interfaces, parameters and functional coverage are release-bound.

IP-3142 · Internal physical evidence · RTL / implementation evaluation

Function and architecture

• Digital RTL implementation indexed as kx_riscv_bpu. The recorded role is risc-v branch prediction; exact interfaces, parameters and functional coverage are release-bound.

• Named source implementation linked to recorded hashed physical outputs.

• Evaluation binds the exact RTL, implementation views and required functional checks; process qualification is not inferred.

Integration summary

KX RISC-V Branch Prediction provides the documented rtl block responsibility: Digital RTL implementation indexed as kx_riscv_bpu. The recorded role is risc-v branch prediction; exact interfaces, parameters and functional coverage are release-bound. Evaluate the exact kx_riscv_bpu implementation and confirm its integration contract before using it inside the target design.

Technical record

Canonical identity	IP-3142
Native implementation identity	kx_riscv_bpu
Documented responsibility	Digital RTL implementation indexed as kx_riscv_bpu. The recorded role is risc-v branch prediction; exact interfaces, parameters and functional coverage are release-bound.
Recorded evidence class	Internal physical evidence
Interface and physical parameters	Bound to the selected source/configuration; not inferred from name or family.

Delivery and release binding

• Exact implementation and configuration manifest

• Documented interfaces and clock/reset contract

• Available reference or verification collateral

• Recorded physical views where authorized and applicable

• Integration acceptance criteria and unresolved gate list

Confirm for the selected release: Source/configuration identity, Interface and dependencies, Verification evidence, Process/library where applicable, Authorized package and acceptance criteria.

Evidence and qualification

Our named implementation inventory records kx_riscv_bpu with hashed GDS output references. Those records are internal physical evidence, not external signoff or verified support for the inventory's node counts.

Evidence shown is our record for this canonical implementation, not a fresh tool rerun. External foundry acceptance, silicon measurements, standards certification and unlisted interface/physical parameters are not inferred. Exact delivery and rights are agreed before licensing.

Canonical status: INTERNAL PHYSICAL RESULT + HASHED GDS; NOT EXTERNAL SIGNOFF

Evaluation and licensing

Evaluation: Review the exact recorded implementation and agreed test scope. Production: Named-design rights for the agreed qualified release. Custom work: Target integration, verification or physical qualification. Rights, pricing, support and acceptance criteria are agreed for the exact scope.

Contact: patrick@garmolabs.com | Product path: /ip/kx-risc-v-branch-prediction-ip-3142