FABRIC & CONNECTIVITY

Garmo-DMA-Engine

Coherent DMA architecture for queued data movement and system integration.

IP-2095 · Evaluation package · Evaluation / IP scope

Function and architecture

- Scatter/gather, chained descriptors, 2D/3D strided copy and tensor swizzle
- 1024+ outstanding transactions with adaptive reordering
- PASID/SVA/IOMMU translation cache and per-context isolation

Integration summary

Garmo-DMA-Engine integration role: System IP — massively parallel coherent DMA fabric. Documented composition: Scatter/gather, chained descriptors, 2D/3D strided copy and tensor swizzle; 1024+ outstanding transactions with adaptive reordering; PASID/SVA/IOMMU translation cache and per-context isolation.

Technical record

Canonical identity	IP-2095
Responsibility	System IP — massively parallel coherent DMA fabric
Documented interface architecture	16 AXI/NoC masters, coherent/IOMMU request path, descriptor fetch, streaming endpoints, IRQ/MSI
Documented building blocks	Scatter/gather, chained descriptors, 2D/3D strided copy and tensor swizzle; 1024+ outstanding transactions with adaptive reordering; PASID/SVA/IOMMU translation cache and per-context isolation
Delivery boundary	Evaluation / IP scope
Evidence scope	Evaluation package
Architecture targets · not measurements	256 logical channels, 16 physical engines, 512-bit datapaths; 1–2 TB/s aggregate internal fabric target at advanced-node clocks.

Delivery and release binding

- Interface version and parameter set
- Clock/reset domains and integration constraints
- Companion memory, PHY and software requirements
- Verification collateral and acceptance criteria

Confirm for the selected release: Node/library binding, Clock/reset limits, Physical and protocol dependencies, Artifact hashes, Acceptance criteria.

Evidence and qualification

Canonical technology and its architecture/integration role are recorded. The offered delivery is confirmed against the exact release before licensing.

No node-port, silicon-performance, standards certification or analog qualification is inherited from a related product.

Canonical status: P0 / REPRESENTATIVE ARCHITECTURE RTL — concrete integration specification and synthesizable RTL shell/representative datapath only; all frequency, throughput, power, area, jitter and standards-superiority figures remain architecture targets until the required evidence hierarchy closes.

Evaluation and licensing

Evaluation: Evaluate an individual IP configuration. Production: Named-design production license. Custom work: Node binding or derivative integration. Rights, pricing, support and acceptance criteria are agreed for the exact scope.

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