INTERFACES & MIXED-SIGNAL

Garmo-PLL-Frac

Mixed Signal — fractional-N / digitally assisted PLL platform

IP-2092 · Evaluation package · Evaluation / IP scope

Function and architecture

- Integer and fractional-N modes with programmable sigma-delta modulator
- Digitally assisted calibration for PVT, gain and loop-bandwidth normalization
- Spread-spectrum clocking, hitless divider changes and glitchless output mux

Integration summary

Garmo-PLL-Frac integration role: Mixed Signal — fractional-N / digitally assisted PLL platform. Documented composition: Integer and fractional-N modes with programmable sigma-delta modulator; Digitally assisted calibration for PVT, gain and loop-bandwidth normalization; Spread-spectrum clocking, hitless divider changes and glitchless output mux.

Technical record

Canonical identity	IP-2092
Responsibility	Mixed Signal — fractional-N / digitally assisted PLL platform
Documented interface architecture	analog VCO/TDC/DAC hard-macro boundaries, refclk, CSR, lock/clock outputs, SSC control
Documented building blocks	Integer and fractional-N modes with programmable sigma-delta modulator; Digitally assisted calibration for PVT, gain and loop-bandwidth normalization; Spread-spectrum clocking, hitless divider changes and glitchless output mux
Delivery boundary	Evaluation / IP scope
Evidence scope	Evaluation package
Architecture targets · not measurements	10 MHz–12 GHz generated output range via VCO/dividers; <300 fs RMS jitter target in high-performance mode; <5 us fast-lock target.

Delivery and release binding

- Interface version and parameter set
- Clock/reset domains and integration constraints
- Companion memory, PHY and software requirements
- Verification collateral and acceptance criteria

Confirm for the selected release: Node/library binding, Clock/reset limits, Physical and protocol dependencies, Artifact hashes, Acceptance criteria.

Evidence and qualification

Canonical technology and its architecture/integration role are recorded. The offered delivery is confirmed against the exact release before licensing.

Control/model IP does not establish analog PHY, electrical, RF or standards compliance. Qualified third-party or foundry collateral may be required.

Canonical status: P3 / REPRESENTATIVE ARCHITECTURE RTL — concrete integration specification and synthesizable RTL shell/representative datapath only; all frequency, throughput, power, area, jitter and standards-superiority figures remain architecture targets until the required evidence hierarchy closes. Analog/custom production claims require transistor-level/custom-layout, extracted PVT/Monte-Carlo and silicon characterization.

Evaluation and licensing

Evaluation: Evaluate an individual IP configuration. Production: Named-design production license. Custom work: Node binding or derivative integration. Rights, pricing, support and acceptance criteria are agreed for the exact scope.

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