MEMORY & STORAGE

Garmo-SRAM-Compiler

Memory IP — node-adaptable SRAM compiler architecture

IP-2091 · Evaluation package · Evaluation / IP scope

Function and architecture

- Bank/word/bit partition search driven by PPA and aspect-ratio constraints
- Redundant row/column repair, MBIST/BISR and SECDED option
- Retention, light/deep sleep, power gating and per-bank clock gating

Integration summary

Garmo-SRAM-Compiler integration role: Memory IP — node-adaptable SRAM compiler architecture. Documented composition: Bank/word/bit partition search driven by PPA and aspect-ratio constraints; Redundant row/column repair, MBIST/BISR and SECDED option; Retention, light/deep sleep, power gating and per-bank clock gating.

Technical record

Canonical identity	IP-2091
Responsibility	Memory IP — node-adaptable SRAM compiler architecture
Documented interface architecture	compiler manifest + generated Verilog model/Liberty/LEF/GDS contract; runtime SRAM ports
Documented building blocks	Bank/word/bit partition search driven by PPA and aspect-ratio constraints; Redundant row/column repair, MBIST/BISR and SECDED option; Retention, light/deep sleep, power gating and per-bank clock gating
Delivery boundary	Evaluation / IP scope
Evidence scope	Evaluation package
Architecture targets · not measurements	64 B to 16 MiB generated macros; 1RW/1R1W/2RW families; ECC/repair/retention options.

Delivery and release binding

- Interface version and parameter set
- Clock/reset domains and integration constraints
- Companion memory, PHY and software requirements
- Verification collateral and acceptance criteria

Confirm for the selected release: Node/library binding, Clock/reset limits, Physical and protocol dependencies, Artifact hashes, Acceptance criteria.

Evidence and qualification

Canonical technology and its architecture/integration role are recorded. The offered delivery is confirmed against the exact release before licensing.

No node-port, silicon-performance, standards certification or analog qualification is inherited from a related product.

Canonical status: P1 / REPRESENTATIVE ARCHITECTURE RTL — concrete integration specification and synthesizable RTL shell/representative datapath only; all frequency, throughput, power, area, jitter and standards-superiority figures remain architecture targets until the required evidence hierarchy closes.

Evaluation and licensing

Evaluation: Evaluate an individual IP configuration. Production: Named-design production license. Custom work: Node binding or derivative integration. Rights, pricing, support and acceptance criteria are agreed for the exact scope.

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