POWER & CONTROL

Garmo-BMS-ADC

Mixed Signal — redundant precision BMS ADC subsystem

IP-2089 · Evaluation package · Evaluation / IP scope

Function and architecture

- Dual-converter cross-check with dissimilar SAR and delta-sigma paths
- 32-cell scan/mux sequencer, open-wire and plausibility diagnostics
- Background offset/gain calibration and temperature compensation

Integration summary

Garmo-BMS-ADC integration role: Mixed Signal — redundant precision BMS ADC subsystem. Documented composition: Dual-converter cross-check with dissimilar SAR and delta-sigma paths; 32-cell scan/mux sequencer, open-wire and plausibility diagnostics; Background offset/gain calibration and temperature compensation.

Technical record

Canonical identity	IP-2089
Responsibility	Mixed Signal — redundant precision BMS ADC subsystem
Documented interface architecture	analog hard-macro sample buses, cell mux controls, SPI/AXI, calibration RAM, safety IRQ
Documented building blocks	Dual-converter cross-check with dissimilar SAR and delta-sigma paths; 32-cell scan/mux sequencer, open-wire and plausibility diagnostics; Background offset/gain calibration and temperature compensation
Delivery boundary	Evaluation / IP scope
Evidence scope	Evaluation package
Architecture targets · not measurements	18-bit SAR fast path to 2 MS/s + 24-bit delta-sigma precision path to 200 kS/s; ±0.5 mV system target after calibration.

Delivery and release binding

- Interface version and parameter set
- Clock/reset domains and integration constraints
- Companion memory, PHY and software requirements
- Verification collateral and acceptance criteria

Confirm for the selected release: Node/library binding, Clock/reset limits, Physical and protocol dependencies, Artifact hashes, Acceptance criteria.

Evidence and qualification

Canonical technology and its architecture/integration role are recorded. The offered delivery is confirmed against the exact release before licensing.

No node-port, silicon-performance, standards certification or analog qualification is inherited from a related product.

Canonical status: P3 / REPRESENTATIVE ARCHITECTURE RTL — concrete integration specification and synthesizable RTL shell/representative datapath only; all frequency, throughput, power, area, jitter and standards-superiority figures remain architecture targets until the required evidence hierarchy closes. Analog/custom production claims require transistor-level/custom-layout, extracted PVT/Monte-Carlo and silicon characterization.

Evaluation and licensing

Evaluation: Evaluate an individual IP configuration. Production: Named-design production license. Custom work: Node binding or derivative integration. Rights, pricing, support and acceptance criteria are agreed for the exact scope.

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