RELIABILITY & SAFETY

Garmo-ASIL-D-Monitor

Safety-monitoring island architecture for fault detection, containment and supervised operation; functional-safety certification is not implied.

IP-2088 · Evaluation package · Evaluation / IP scope

Function and architecture

- Dual-diverse safety sequencers with temporal lockstep option
- ECC/parity aggregation, periodic SRAM scrub and register CRC
- Windowed watchdogs, clock/power plausibility and heartbeat matrix

Integration summary

Garmo-ASIL-D-Monitor integration role: Safety — ASIL-D safety island / monitor. Documented composition: Dual-diverse safety sequencers with temporal lockstep option; ECC/parity aggregation, periodic SRAM scrub and register CRC; Windowed watchdogs, clock/power plausibility and heartbeat matrix.

Technical record

Canonical identity	IP-2088
Responsibility	Safety — ASIL-D safety island / monitor
Documented interface architecture	fault event fabric, lockstep compare, watchdogs, clock/power sensors, safe-state outputs, CSR
Documented building blocks	Dual-diverse safety sequencers with temporal lockstep option; ECC/parity aggregation, periodic SRAM scrub and register CRC; Windowed watchdogs, clock/power plausibility and heartbeat matrix
Delivery boundary	Evaluation / IP scope
Evidence scope	Evaluation package
Architecture targets · not measurements	SPFM >99%, LFM >90% design goals; <10 us critical fault-to-safe-request target.

Delivery and release binding

- Interface version and parameter set
- Clock/reset domains and integration constraints
- Companion memory, PHY and software requirements
- Verification collateral and acceptance criteria

Confirm for the selected release: Node/library binding, Clock/reset limits, Physical and protocol dependencies, Artifact hashes, Acceptance criteria.

Evidence and qualification

Canonical technology and its architecture/integration role are recorded. The offered delivery is confirmed against the exact release before licensing.

No node-port, silicon-performance, standards certification or analog qualification is inherited from a related product.

Canonical status: P0 / REPRESENTATIVE ARCHITECTURE RTL — concrete integration specification and synthesizable RTL shell/representative datapath only; all frequency, throughput, power, area, jitter and standards-superiority figures remain architecture targets until the required evidence hierarchy closes.

Evaluation and licensing

Evaluation: Evaluate an individual IP configuration. Production: Named-design production license. Custom work: Node binding or derivative integration. Rights, pricing, support and acceptance criteria are agreed for the exact scope.

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