MEMORY & STORAGE

Garmo-LPDDR5X-MC

Low-power DRAM controller architecture with scheduling and external PHY integration.

IP-2080 · Evaluation package · Evaluation / IP scope

Function and architecture

- WCK management, command bus training and read/write leveling orchestration
- Deep power-down, self-refresh, partial-array self-refresh and per-bank refresh
- Latency-aware QoS for CPU/GPU/NPU mixed traffic

Integration summary

Garmo-LPDDR5X-MC integration role: Memory — 10.7 Gb/s LPDDR5X controller. Documented composition: WCK management, command bus training and read/write leveling orchestration; Deep power-down, self-refresh, partial-array self-refresh and per-bank refresh; Latency-aware QoS for CPU/GPU/NPU mixed traffic.

Technical record

Canonical identity	IP-2080
Responsibility	Memory — 10.7 Gb/s LPDDR5X controller
Documented interface architecture	AXI/NoC, DFI-like LPDDR PHY, PMU and thermal interface
Documented building blocks	WCK management, command bus training and read/write leveling orchestration; Deep power-down, self-refresh, partial-array self-refresh and per-bank refresh; Latency-aware QoS for CPU/GPU/NPU mixed traffic
Delivery boundary	Evaluation / IP scope
Evidence scope	Evaluation package
Architecture targets · not measurements	4 controller instances, x16 channels, 10.7 Gb/s/pin qualified target, DVFS with sub-microsecond policy transition.

Delivery and release binding

- Interface version and parameter set
- Clock/reset domains and integration constraints
- Companion memory, PHY and software requirements
- Verification collateral and acceptance criteria

Confirm for the selected release: Node/library binding, Clock/reset limits, Physical and protocol dependencies, Artifact hashes, Acceptance criteria.

Evidence and qualification

Canonical technology and its architecture/integration role are recorded. The offered delivery is confirmed against the exact release before licensing.

No node-port, silicon-performance, standards certification or analog qualification is inherited from a related product.

Canonical status: P2 / REPRESENTATIVE ARCHITECTURE RTL — concrete integration specification and synthesizable RTL shell/representative datapath only; all frequency, throughput, power, area, jitter and standards-superiority figures remain architecture targets until the required evidence hierarchy closes. Electrical/PHY production claims require a characterized foundry/node hard-macro backend plus package/channel and compliance evidence.

Evaluation and licensing

Evaluation: Evaluate an individual IP configuration. Production: Named-design production license. Custom work: Node binding or derivative integration. Rights, pricing, support and acceptance criteria are agreed for the exact scope.

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