MEMORY & STORAGE

Garmo-DDR5-MC

Memory — high-throughput DDR5 controller

IP-2079 · Evaluation package · Evaluation / IP scope

Function and architecture

- FR-FCFS/QoS scheduler with row locality and deadline classes
- Per-bank refresh, refresh postponement/pull-in and thermal throttling
- SECDED/Chipkill-style system ECC hooks, patrol scrub, poison containment

Integration summary

Garmo-DDR5-MC integration role: Memory — high-throughput DDR5 controller. Documented composition: FR-FCFS/QoS scheduler with row locality and deadline classes; Per-bank refresh, refresh postponement/pull-in and thermal throttling; SECDED/Chipkill-style system ECC hooks, patrol scrub, poison containment.

Technical record

Canonical identity	IP-2079
Responsibility	Memory — high-throughput DDR5 controller
Documented interface architecture	AXI4/NoC front side, DFI-like PHY interface, RAS/interrupt/PMU
Documented building blocks	FR-FCFS/QoS scheduler with row locality and deadline classes; Per-bank refresh, refresh postponement/pull-in and thermal throttling; SECDED/Chipkill-style system ECC hooks, patrol scrub, poison containment
Delivery boundary	Evaluation / IP scope
Evidence scope	Evaluation package
Architecture targets · not measurements	Up to 8 controllers × 2 subchannels; 8.8–9.6 GT/s PHY-ready target; >90% sustained bandwidth on streaming.

Delivery and release binding

- Interface version and parameter set
- Clock/reset domains and integration constraints
- Companion memory, PHY and software requirements
- Verification collateral and acceptance criteria

Confirm for the selected release: Node/library binding, Clock/reset limits, Physical and protocol dependencies, Artifact hashes, Acceptance criteria.

Evidence and qualification

Canonical technology and its architecture/integration role are recorded. The offered delivery is confirmed against the exact release before licensing.

No node-port, silicon-performance, standards certification or analog qualification is inherited from a related product.

Canonical status: P2 / REPRESENTATIVE ARCHITECTURE RTL — concrete integration specification and synthesizable RTL shell/representative datapath only; all frequency, throughput, power, area, jitter and standards-superiority figures remain architecture targets until the required evidence hierarchy closes. Electrical/PHY production claims require a characterized foundry/node hard-macro backend plus package/channel and compliance evidence.

Evaluation and licensing

Evaluation: Evaluate an individual IP configuration. Production: Named-design production license. Custom work: Node binding or derivative integration. Rights, pricing, support and acceptance criteria are agreed for the exact scope.

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