INTERFACES & MIXED-SIGNAL

Garmo-PCIe-5.0-PHY

PCIe controller and PHY-control integration architecture, with protocol and electrical qualification scoped to the exact release.

IP-2076 · Evaluation package · Evaluation / IP scope

Function and architecture

- PAM4 Gen6/7 FLIT mode, CRC/FEC orchestration and replay
- Lane bifurcation, polarity reversal, lane reversal and degraded-width operation
- LTSSM with margining, equalization and autonomous recovery

Integration summary

Garmo-PCIe-5.0-PHY integration role: High-Speed I/O — PCIe 7.0-capable controller/PCS/PMA-control subsystem. Documented composition: PAM4 Gen6/7 FLIT mode, CRC/FEC orchestration and replay; Lane bifurcation, polarity reversal, lane reversal and degraded-width operation; LTSSM with margining, equalization and autonomous recovery.

Technical record

Canonical identity	IP-2076
Responsibility	High-Speed I/O — PCIe 7.0-capable controller/PCS/PMA-control subsystem
Documented interface architecture	PIPE-like PHY boundary, AXI streaming transaction side, APB/CSR, sideband/reset/refclk
Documented building blocks	PAM4 Gen6/7 FLIT mode, CRC/FEC orchestration and replay; Lane bifurcation, polarity reversal, lane reversal and degraded-width operation; LTSSM with margining, equalization and autonomous recovery
Delivery boundary	Evaluation / IP scope
Evidence scope	Evaluation package
Architecture targets · not measurements	Gen1–Gen7, 2.5–128 GT/s per lane, x1–x16; 512 GB/s bidirectional raw at x16 Gen7.

Delivery and release binding

- Interface version and parameter set
- Clock/reset domains and integration constraints
- Companion memory, PHY and software requirements
- Verification collateral and acceptance criteria

Confirm for the selected release: Node/library binding, Clock/reset limits, Physical and protocol dependencies, Artifact hashes, Acceptance criteria.

Evidence and qualification

Canonical technology and its architecture/integration role are recorded. The offered delivery is confirmed against the exact release before licensing.

Control/model IP does not establish analog PHY, electrical, RF or standards compliance. Qualified third-party or foundry collateral may be required.

Canonical status: P2 / REPRESENTATIVE ARCHITECTURE RTL — concrete integration specification and synthesizable RTL shell/representative datapath only; all frequency, throughput, power, area, jitter and standards-superiority figures remain architecture targets until the required evidence hierarchy closes. Electrical/PHY production claims require a characterized foundry/node hard-macro backend plus package/channel and compliance evidence.

Evaluation and licensing

Evaluation: Evaluate an individual IP configuration. Production: Named-design production license. Custom work: Node binding or derivative integration. Rights, pricing, support and acceptance criteria are agreed for the exact scope.

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