COMPUTE & AI

Garmo-RV64-GC

CPU — maximum-performance RISC-V core

IP-2073 · Evaluation package · Evaluation / IP scope

Function and architecture

- 8-wide fetch/decode/rename with micro-op cache
- 14–16 issue backend, 512 ROB, 256 load/store entries, 4 AGUs
- Dual 512-bit RVV/vector-crypto pipelines with matrix-assist custom extension hooks

Integration summary

Garmo-RV64-GC integration role: CPU — maximum-performance RISC-V core. Documented composition: 8-wide fetch/decode/rename with micro-op cache; 14–16 issue backend, 512 ROB, 256 load/store entries, 4 AGUs; Dual 512-bit RVV/vector-crypto pipelines with matrix-assist custom extension hooks.

Technical record

Canonical identity	IP-2073
Responsibility	CPU — maximum-performance RISC-V core
Documented interface architecture	Coherent mesh/CHI-compatible bridge, 1024-bit L3 fabric, CXL/UCIe coherent agent hooks
Documented building blocks	8-wide fetch/decode/rename with micro-op cache; 14–16 issue backend, 512 ROB, 256 load/store entries, 4 AGUs; Dual 512-bit RVV/vector-crypto pipelines with matrix-assist custom extension hooks
Delivery boundary	Evaluation / IP scope
Evidence scope	Evaluation package
Architecture targets · not measurements	8-wide OoO, 512-entry ROB, dual 512-bit vector, SMT2 option; >2.2 SPECint2017/GHz target.

Delivery and release binding

- Interface version and parameter set
- Clock/reset domains and integration constraints
- Companion memory, PHY and software requirements
- Verification collateral and acceptance criteria

Confirm for the selected release: Node/library binding, Clock/reset limits, Physical and protocol dependencies, Artifact hashes, Acceptance criteria.

Evidence and qualification

Canonical technology and its architecture/integration role are recorded. The offered delivery is confirmed against the exact release before licensing.

No node-port, silicon-performance, standards certification or analog qualification is inherited from a related product.

Canonical status: P0 / REPRESENTATIVE ARCHITECTURE RTL — concrete integration specification and synthesizable RTL shell/representative datapath only; all frequency, throughput, power, area, jitter and standards-superiority figures remain architecture targets until the required evidence hierarchy closes.

Evaluation and licensing

Evaluation: Evaluate an individual IP configuration. Production: Named-design production license. Custom work: Node binding or derivative integration. Rights, pricing, support and acceptance criteria are agreed for the exact scope.

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