COMPUTE & AI

Garmo-RV32-EC

CPU — high-efficiency RISC-V MCU core

IP-2071 · Evaluation package · Evaluation / IP scope

Function and architecture

- 2-wide fetch/decode with decoupled branch unit and 16-entry return stack
- Physical memory protection, machine/user modes, optional MMU-lite
- 32/64 KiB I/D cache options or deterministic TCM

Integration summary

Garmo-RV32-EC integration role: CPU — high-efficiency RISC-V MCU core. Documented composition: 2-wide fetch/decode with decoupled branch unit and 16-entry return stack; Physical memory protection, machine/user modes, optional MMU-lite; 32/64 KiB I/D cache options or deterministic TCM.

Technical record

Canonical identity	IP-2071
Responsibility	CPU — high-efficiency RISC-V MCU core
Documented interface architecture	Harvard I/D memory, AXI/AHB adapter, debug, CLINT/PLIC/AIA option, TCM
Documented building blocks	2-wide fetch/decode with decoupled branch unit and 16-entry return stack; Physical memory protection, machine/user modes, optional MMU-lite; 32/64 KiB I/D cache options or deterministic TCM
Delivery boundary	Evaluation / IP scope
Evidence scope	Evaluation package
Architecture targets · not measurements	RV32IMAFDCB + optional 128-bit V; 2-wide in-order; >6 CoreMark/MHz target; <12-cycle interrupt entry.

Delivery and release binding

- Interface version and parameter set
- Clock/reset domains and integration constraints
- Companion memory, PHY and software requirements
- Verification collateral and acceptance criteria

Confirm for the selected release: Node/library binding, Clock/reset limits, Physical and protocol dependencies, Artifact hashes, Acceptance criteria.

Evidence and qualification

Canonical technology and its architecture/integration role are recorded. The offered delivery is confirmed against the exact release before licensing.

No node-port, silicon-performance, standards certification or analog qualification is inherited from a related product.

Canonical status: P0 / REPRESENTATIVE ARCHITECTURE RTL — concrete integration specification and synthesizable RTL shell/representative datapath only; all frequency, throughput, power, area, jitter and standards-superiority figures remain architecture targets until the required evidence hierarchy closes.

Evaluation and licensing

Evaluation: Evaluate an individual IP configuration. Production: Named-design production license. Custom work: Node binding or derivative integration. Rights, pricing, support and acceptance criteria are agreed for the exact scope.

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