COMPUTE & AI

Garmo-VEC-DSP

AI/DSP Compute — 1024-bit deterministic vector DSP

IP-2068 · Evaluation package · Evaluation / IP scope

Function and architecture

- 1024-bit vector register file with 64 architectural vectors
- INT8/16/32, FP16/BF16/FP32, complex MAC, saturating/fixed-point arithmetic
- FFT butterfly, FIR, dot-product, permute, gather/scatter primitives

Integration summary

Garmo-VEC-DSP integration role: AI/DSP Compute — 1024-bit deterministic vector DSP. Documented composition: 1024-bit vector register file with 64 architectural vectors; INT8/16/32, FP16/BF16/FP32, complex MAC, saturating/fixed-point arithmetic; FFT butterfly, FIR, dot-product, permute, gather/scatter primitives.

Technical record

Canonical identity	IP-2068
Responsibility	AI/DSP Compute — 1024-bit deterministic vector DSP
Documented interface architecture	AXI4 256-bit, AXI4-Lite CSR, streaming I/Q ports, DMA request/response, IRQ
Documented building blocks	1024-bit vector register file with 64 architectural vectors; INT8/16/32, FP16/BF16/FP32, complex MAC, saturating/fixed-point arithmetic; FFT butterfly, FIR, dot-product, permute, gather/scatter primitives
Delivery boundary	Evaluation / IP scope
Evidence scope	Evaluation package
Architecture targets · not measurements	4 vector pipes, 1024-bit vectors, 2.0 GHz target; 16.4 TOPS INT8 MAC peak; <20-cycle interrupt-to-vector service.

Delivery and release binding

- Interface version and parameter set
- Clock/reset domains and integration constraints
- Companion memory, PHY and software requirements
- Verification collateral and acceptance criteria

Confirm for the selected release: Node/library binding, Clock/reset limits, Physical and protocol dependencies, Artifact hashes, Acceptance criteria.

Evidence and qualification

Canonical technology and its architecture/integration role are recorded. The offered delivery is confirmed against the exact release before licensing.

No node-port, silicon-performance, standards certification or analog qualification is inherited from a related product.

Canonical status: P1 / REPRESENTATIVE ARCHITECTURE RTL — concrete integration specification and synthesizable RTL shell/representative datapath only; all frequency, throughput, power, area, jitter and standards-superiority figures remain architecture targets until the required evidence hierarchy closes.

Evaluation and licensing

Evaluation: Evaluate an individual IP configuration. Production: Named-design production license. Custom work: Node binding or derivative integration. Rights, pricing, support and acceptance criteria are agreed for the exact scope.

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