MEMORY & COHERENCY

Reconstructible Memory Controller

Reconstruction-recipe memory controller with integrity gating

IP-2016 · Executed digital evidence · RTL / reference evaluation

Function and architecture

• RTL exists

• 74/0 simulation

• BMC + induction proved

• generic synthesis top reported at 83,310 cells. Cross-links GMF/GSN-GMA/Continuum without replacing them

Integration summary

Reconstructible Memory Controller provides the documented reconstruction-recipe memory controller with integrity gating responsibility: Reconstruction-recipe memory controller with integrity gating Evaluate the exact IP-2016 implementation and confirm its integration contract before using it inside the target design.

Technical record

Canonical identity	IP-2016
Native implementation identity	IP-2016
Documented responsibility	Reconstruction-recipe memory controller with integrity gating
Recorded evidence class	Executed digital evidence
Interface and physical parameters	Bound to the selected source/configuration; not inferred from name or family.

Delivery and release binding

• Exact implementation and configuration manifest

• Documented interfaces and clock/reset contract

• Available reference or verification collateral

• Recorded physical views where authorized and applicable

• Integration acceptance criteria and unresolved gate list

Confirm for the selected release: Source/configuration identity, Interface and dependencies, Verification evidence, Process/library where applicable, Authorized package and acceptance criteria.

Evidence and qualification

RTL exists; 74/0 simulation; BMC + induction proved; generic synthesis top reported at 83,310 cells. Cross-links GMF/GSN-GMA/Continuum without replacing them.

Evidence shown is our record for this canonical implementation, not a fresh tool rerun. External foundry acceptance, silicon measurements, standards certification and unlisted interface/physical parameters are not inferred. Exact delivery and rights are agreed before licensing.

Canonical status: RTL + SIMULATION + FORMAL INDUCTION + GENERIC SYNTHESIS EVIDENCED — no physical implementation or silicon evidence.

Evaluation and licensing

Evaluation: Review the exact recorded implementation and agreed test scope. Production: Named-design rights for the agreed qualified release. Custom work: Target integration, verification or physical qualification. Rights, pricing, support and acceptance criteria are agreed for the exact scope.

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