INTEGRATION & TOOLING

GST — Silicon Test Platform

Manufacturing/post-silicon test, characterization, diagnostics and test evidence

IP-149 · Architecture IP · Architecture

Function and architecture

- Manufacturing/post-silicon test
- characterization
- diagnostics and test evidence

Integration summary

GST — Silicon Test Platform integration role: Silicon test platform. Documented composition: Manufacturing/post-silicon test, characterization, diagnostics and test evidence.

Technical record

Canonical identity	IP-149
Responsibility	Silicon test platform
Documented building blocks	Manufacturing/post-silicon test, characterization, diagnostics and test evidence
Delivery boundary	Architecture
Evidence scope	Architecture IP

Delivery and release binding

- Interface version and parameter set
- Clock/reset domains and integration constraints
- Companion memory, PHY and software requirements
- Verification collateral and acceptance criteria

Confirm for the selected release: Node/library binding, Clock/reset limits, Physical and protocol dependencies, Artifact hashes, Acceptance criteria.

Evidence and qualification

Canonical technology and its architecture/integration role are recorded. The offered delivery is confirmed against the exact release before licensing.

No node-port, silicon-performance, standards certification or analog qualification is inherited from a related product.

Canonical status: Master build spec; acronym collision

Evaluation and licensing

Evaluation: Evaluate an individual IP configuration. Production: Named-design production license. Custom work: Node binding or derivative integration. Rights, pricing, support and acceptance criteria are agreed for the exact scope.

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