MEMORY & STORAGE

GMA — Memory Architecture

Memory attributes, ordering, cacheability, atomics, DMA/coherency, NUMA, ECC, poison, scrub, encryption hooks

IP-121 · Architecture IP · Architecture

Function and architecture

- Memory attributes
- ordering
- cacheability
- atomics
- DMA/coherency
- poison
- scrub

Integration summary

GMA — Memory Architecture integration role: Technology-neutral memory architecture. Documented composition: Memory attributes, ordering, cacheability, atomics, DMA/coherency, NUMA, ECC, poison, scrub, encryption hooks.

Technical record

Canonical identity	IP-121
Responsibility	Technology-neutral memory architecture
Documented building blocks	Memory attributes, ordering, cacheability, atomics, DMA/coherency, NUMA, ECC, poison, scrub, encryption hooks
Delivery boundary	Architecture
Evidence scope	Architecture IP

Delivery and release binding

- Interface version and parameter set
- Clock/reset domains and integration constraints
- Companion memory, PHY and software requirements
- Verification collateral and acceptance criteria

Confirm for the selected release: Node/library binding, Clock/reset limits, Physical and protocol dependencies, Artifact hashes, Acceptance criteria.

Evidence and qualification

Canonical technology and its architecture/integration role are recorded. The offered delivery is confirmed against the exact release before licensing.

No node-port, silicon-performance, standards certification or analog qualification is inherited from a related product.

Canonical status: Engineering architecture

Evaluation and licensing

Evaluation: Evaluate an individual IP configuration. Production: Named-design production license. Custom work: Node binding or derivative integration. Rights, pricing, support and acceptance criteria are agreed for the exact scope.

Contact: patrick@garmolabs.com | Product path: /ip/gma-memory-architecture