COMPUTE & AI

Garmo RISC-V Processor IP

CPU pipeline; cache/memory interfaces; MMU/TLB options; interrupt/debug; FPU/vector options; compiler/software support; verification/formal collateral; hardened physical views.

IP-001 · Architecture IP · Architecture

Function and architecture

- CPU pipeline
- cache/memory interfaces
- MMU/TLB options
- interrupt/debug
- FPU/vector options
- compiler/software support
- verification/formal collateral

Integration summary

Garmo RISC-V Processor IP integration role: CPU core / processor subsystem. Documented composition: CPU pipeline; cache/memory interfaces; MMU/TLB options; interrupt/debug; FPU/vector options; compiler/software support; verification/formal collateral; hardened physical views..

Technical record

Canonical identity	IP-001
Responsibility	CPU core / processor subsystem
Documented building blocks	CPU pipeline; cache/memory interfaces; MMU/TLB options; interrupt/debug; FPU/vector options; compiler/software support; verification/formal collateral; hardened physical views.
Delivery boundary	Architecture
Evidence scope	Architecture IP

Delivery and release binding

- Interface version and parameter set
- Clock/reset domains and integration constraints
- Companion memory, PHY and software requirements
- Verification collateral and acceptance criteria

Confirm for the selected release: Node/library binding, Clock/reset limits, Physical and protocol dependencies, Artifact hashes, Acceptance criteria.

Evidence and qualification

Canonical technology and its architecture/integration role are recorded. The offered delivery is confirmed against the exact release before licensing.

No node-port, silicon-performance, standards certification or analog qualification is inherited from a related product.

Canonical status: Engineering build-spec family

Evaluation and licensing

Evaluation: Evaluate an individual IP configuration. Production: Named-design production license. Custom work: Node binding or derivative integration. Rights, pricing, support and acceptance criteria are agreed for the exact scope.

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